METHODS FOR CHARACTERIZING, GENERATING TEST SEQUENCES FOR, AND/OR SIMULATING INTEGRATED CIRCUIT FAULTS USING FAULT TUPLES AND RELATED SYSTEMS AND COMPUTER PROGRAM PRODUCTS

ABSTRACT

A fault in an integrated circuit device can be characterized using fault tuples. In particular, an integrated circuit device can include primary inputs, primary outputs, and a plurality of signal lines and circuits interconnecting the primary inputs and outputs. A fault tuple is defined to include an identification of a signal line, a signal line value, and a clock cycle constraint for the signal line. A fault tuple is satisfied by providing a test sequence comprising one or more test patterns such that the signal line is controlled to the signal line value during a clock cycle of the test sequence defined by the clock cycle constraint responsive to application of the test sequence to the primary inputs. Fault tuples can be used to generate and simulate test sequences.